6809 AND 6810

DABiC-IV, 10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS

A6810xA
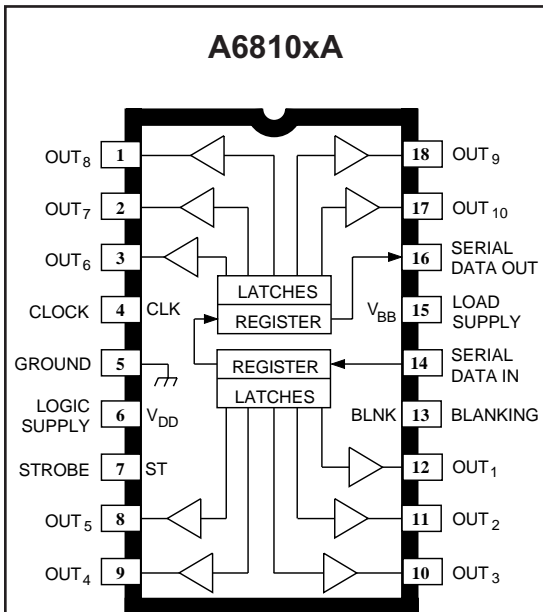
Dwg. PP-029

ABSOLUTE MAXIMUM RATINGS
at T_A = 25°C

Logic Supply Voltage, V_{DD} .... **7.0 V**
Driver Supply Voltage, V_{BB} .... **60 V**
Continuous Output Current Range,
   I_{OUT} .... **-40 mA to +15 mA**
Input Voltage Range,
   V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**
Package Power Dissipation,
   P_D .... **See Graph**
Operating Temperature Range, T_A
   (Suffix 'E–') .... **-40°C to +85°C**
   (Suffix 'K–') .... **-40°C to +125°C**
   (Suffix 'S–') .... **-20°C to +85°C**
Storage Temperature Range,
   T_S .... **-55°C to +125°C**

Caution: These CMOS devices have input static protection (Class 2) but are still susceptible to damage if exposed to extremely high static electrical charges.

The A6809– and A6810– devices combine 10-bit CMOS shift registers, accompanying data latches and control circuitry with bipolar sourcing outputs and pnp active pull downs. Designed primarily to drive vacuum-fluorescent displays, the 60 V and -40 mA output ratings also allow these devices to be used in many other peripheral power driver applications. The A6809– and A6810– feature an increased data input rate (compared with the older UCN/UCQ5810-F) and a controlled output slew rate. The A6809xLW and A6810xLW are identical except for pinout.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. With a 3.3 V or 5 V logic supply, typical serial-data input rates are up to 33 MHz.

A CMOS serial data output permits cascade connections in applications requiring additional drive lines. Similar devices are available as the A6811– (12 bits), A6812– (20 bits), and A6818– (32 bits).

The A6809– and A6810– output source drivers are npn Darlingtons, capable of sourcing up to 40 mA. The controlled output slew rate reduces electromagnetic noise, which is an important consideration in systems that include telecommunications and/or microprocessors and to meet government emissions regulations. For inter-digit blanking, all output drivers can be disabled and all sink drivers turned on with a BLANKING input high. The pnp active pull-downs will sink at least 2.5 mA.

Th A6810– is available in three temperature ranges for optimum performance in commercial (suffix S-), industrial (suffix E-), or automotive (suffix K-) applications; package styles are provided for through-hole DIP (suffix -A), surface-mount SOIC (suffix -LW), or minimum-area surface-mount PLCC (suffix -EP). The A6809– is provided in the commercial or industrial temperature ranges and in the SOIC package (suffixes SLW or ELW) only. Copper lead frames, low logic-power dissipation, and low output-saturation voltages allow all devices to source 25 mA from all outputs continuously at 85°C or more than 5 mA over the maximum operating temperature range.

FEATURES

- Controlled Output Slew Rate
- High-Speed Data Storage
- 60 V Minimum Output Breakdown
- High Data Input Rate
- PNP Active Pull-Downs
- Low Output-Saturation Voltages
- Low-Power CMOS Logic and Latches
- Improved Replacements for TL4810–, UCN5810–, and UCQ5810–

Complete part number includes a suffix to identify operating temperature range (E-, K-, or S-) and package type (-A, -EP, or -LW). Always order by complete part number, e.g., **A6810SLW** .
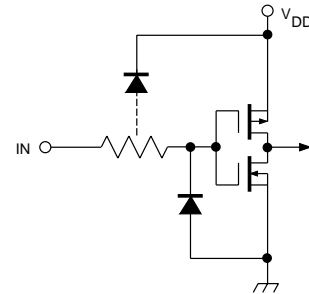
Allegro MicroSystems, Inc.

TYPICAL OUTPUT DRIVER
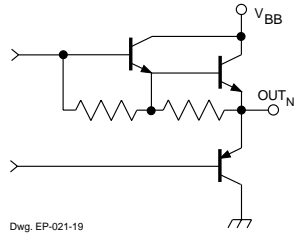
Dwg. EP-021-19

TYPICAL INPUT CIRCUIT

Dwg. EP-010-5

A6809ELW and A6809SLW
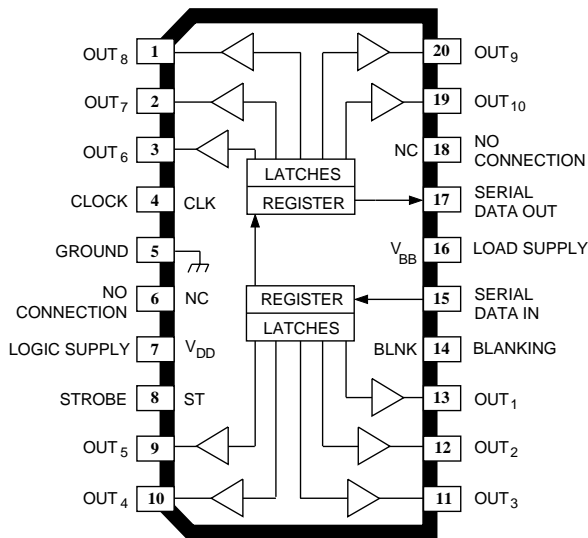
Dwg. PP-029-9

A6810xEP
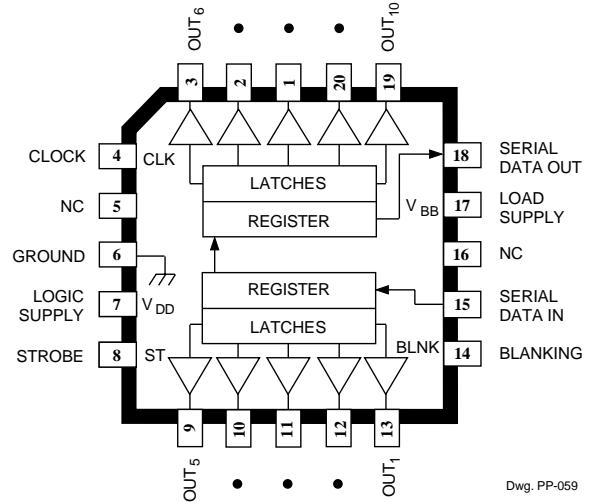
Dwg. PP-059

A6810xLW
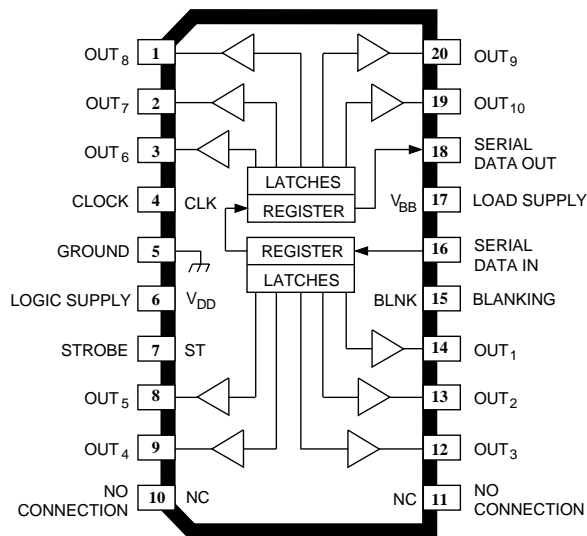
Dwg. PP-029-2

Dwg. GP-024-1

FUNCTIONAL BLOCK DIAGRAM

Dwg. FP-013-1
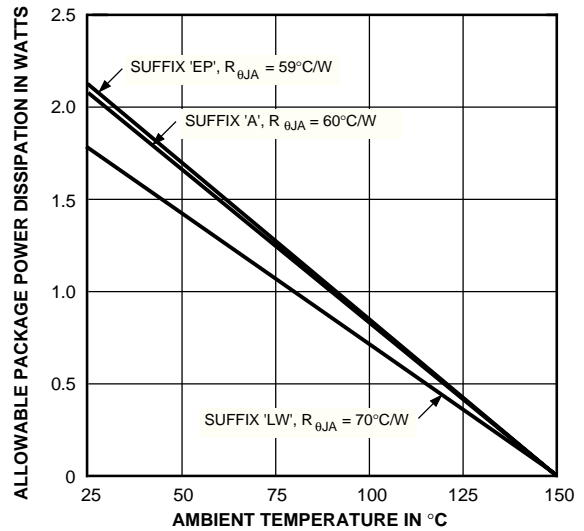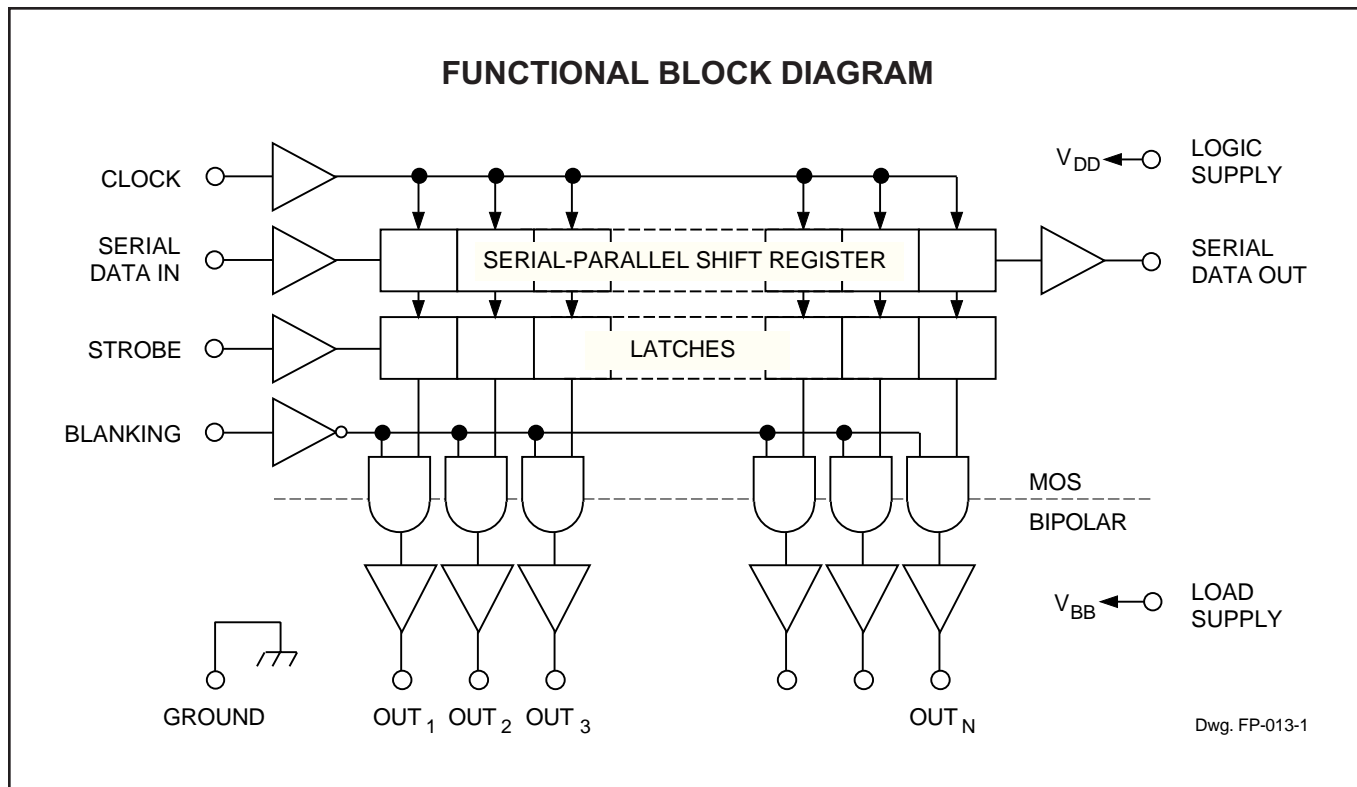
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Blanking	Output Contents					
		I_1	I_2	I_3	...	I_{N-1}	I_N			I_1	I_2	I_3	...	I_{N-1}	I_N		I_1	I_2	I_3	...	I_{N-1}	I_N
H	⌐‾	H	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
L	⌐‾	L	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
X	‾⌐	R_1	R_2	R_3	...	R_{N-1}	R_N	R_N														
		X	X	X	...	X	X	X	L	R_1	R_2	R_3	...	R_{N-1}	R_N							
		P_1	P_2	P_3	...	P_{N-1}	P_N	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N	L	P_1	P_2	P_3	...	P_{N-1}	P_N
										X	X	X	...	X	X	H	L	L	L	...	L	L

L = Low Logic Level   H = High Logic Level   X = Irrelevant   P = Present State   R = Previous State

ELECTRICAL CHARACTERISTICS at T_A = +25°C (A6809SLW & A6810S-) or over operating temperature range (A6809ELW, A6810E-, & A6810K-), V_{BB} = 60 V unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 3.3 V			Limits @ V_{DD} = 5 V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V	—	<-0.1	-15	—	<-0.1	-15	μA
Output Voltage	$V_{OUT(1)}$	I_{OUT} = -25 mA	57.5	58.3	—	57.5	58.3	—	V
	$V_{OUT(0)}$	I_{OUT} = 1 mA	—	1.0	1.5	—	1.0	1.5	V
Output Pull-Down Current	$I_{OUT(0)}$	V_{OUT} = 5 V to V_{BB}	2.5	5.0	—	2.5	5.0	—	mA
Input Voltage	$V_{IN(1)}$		2.2	—	—	3.3	—	—	V
	$V_{IN(0)}$		—	—	1.1	—	—	1.7	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	<0.01	1.0	—	<0.01	1.0	μA
	$I_{IN(0)}$	V_{IN} = 0 V	—	<-0.01	-1.0	—	<-0.01	-1.0	μA
Input Clamp Voltage	V_{IK}	I_{IN} = -200 μA	—	-0.8	-1.5	—	-0.8	-1.5	V
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 μA	2.8	3.05	—	4.5	4.75	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 μA	—	0.15	0.3	—	0.15	0.3	V
Maximum Clock Frequency	f_c		10	33	—	10	33	—	MHz
Logic Supply Current	$I_{DD(1)}$	All Outputs High	—	0.25	0.75	—	0.3	1.0	mA
	$I_{DD(0)}$	All Outputs Low	—	0.25	0.75	—	0.3	1.0	mA
Load Supply Current	$I_{BB(1)}$	All Outputs High, No Load	—	1.5	3.0	—	1.5	3.0	mA
	$I_{BB(0)}$	All Outputs Low	—	0.2	20	—	0.2	20	μA
Blanking-to-Output Delay	$t_{dis(BQ)}$	C_L = 30 pF, 50% to 50%	—	0.7	2.0	—	0.7	2.0	μs
	$t_{en(BQ)}$	C_L = 30 pF, 50% to 50%	—	1.8	3.0	—	1.8	3.0	μs
Strobe-to-Output Delay	$t_{p(STH-QL)}$	R_L = 2.3 kΩ, C_L ≤ 30 pF	—	0.7	2.0	—	0.7	2.0	μs
	$t_{p(STH-QH)}$	R_L = 2.3 kΩ, C_L ≤ 30 pF	—	1.8	3.0	—	1.8	3.0	μs
Output Fall Time	t_f	R_L = 2.3 kΩ, C_L ≤ 30 pF	2.4	—	12	2.4	—	12	μs
Output Rise Time	t_r	R_L = 2.3 kΩ, C_L ≤ 30 pF	2.4	—	12	2.4	—	12	μs
Output Slew Rate	dV/dt	R_L = 2.3 kΩ, C_L ≤ 30 pF	4.0	—	20	4.0	—	20	V/μs
Clock-to-Serial Data Out Delay	$t_{p(CH-SQX)}$	I_{OUT} = ±200 μA	—	50	—	—	50	—	ns

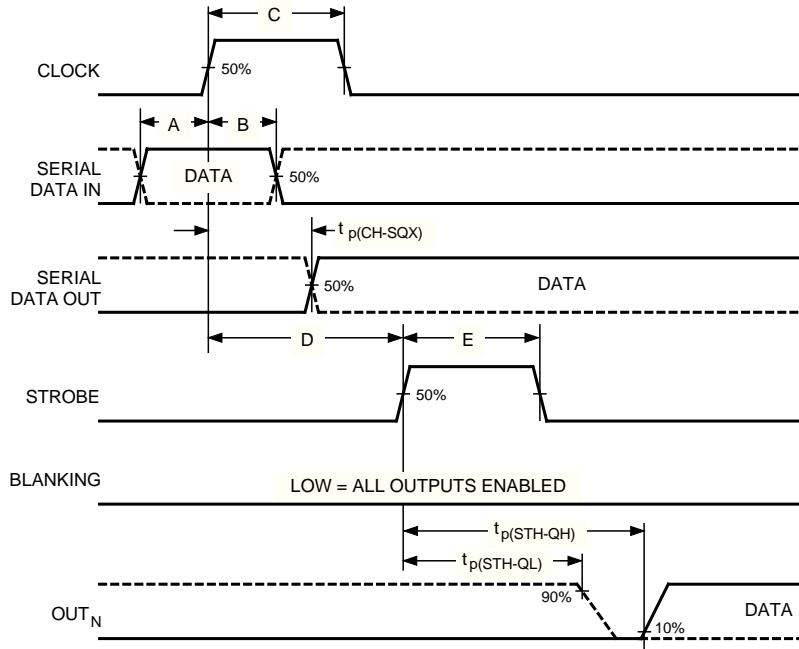Negative current is defined as coming out of (sourcing) the specified device terminal.

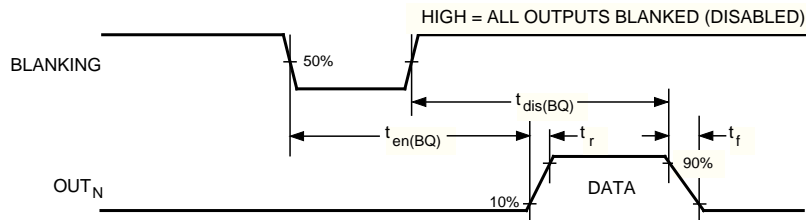Typical data is is for design information only and is at T_A = +25°C.

TIMING REQUIREMENTS and SPECIFICATIONS
(Logic Levels are V_{DD} and Ground)

Dwg. WP-029

Dwg. WP-030

A. Data Active Time Before Clock Pulse
(Data Set-Up Time), $t_{su(D)}$ .... **25 ns**

B. Data Active Time After Clock Pulse
(Data Hold Time), $t_{h(D)}$ .... **25 ns**

C. Clock Pulse Width, $t_{w(CH)}$ .... **50 ns**

D. Time Between Clock Activation and Strobe, $t_{su(C)}$ .... **100 ns**

E. Strobe Pulse Width, $t_{w(STH)}$ .... **50 ns**

NOTE – Timing is representative of a 10 MHz clock. Significantly higher speeds are attainable.

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.
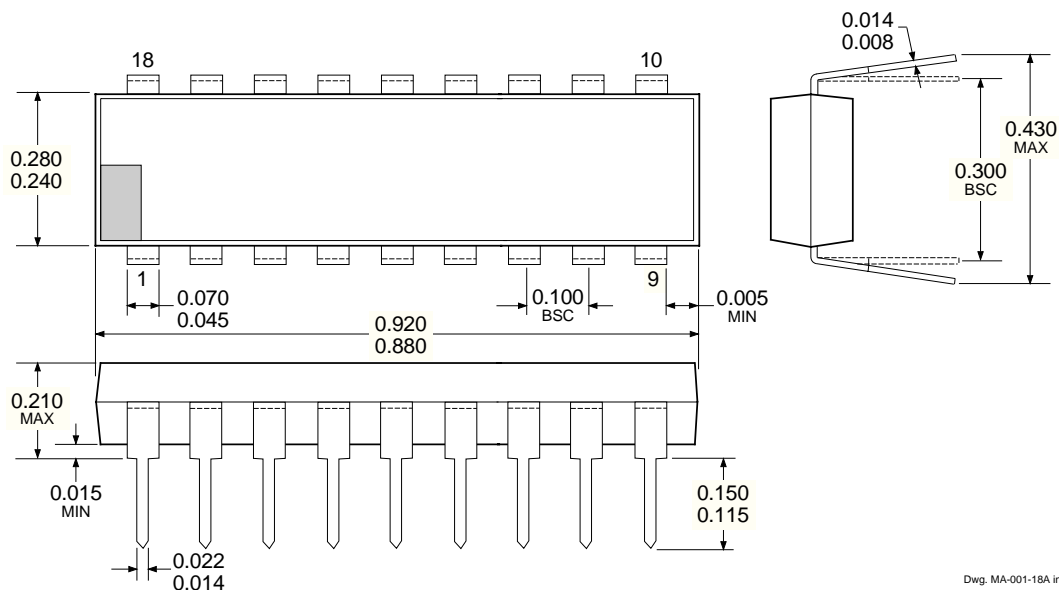
Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the pnp active pull-down sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.
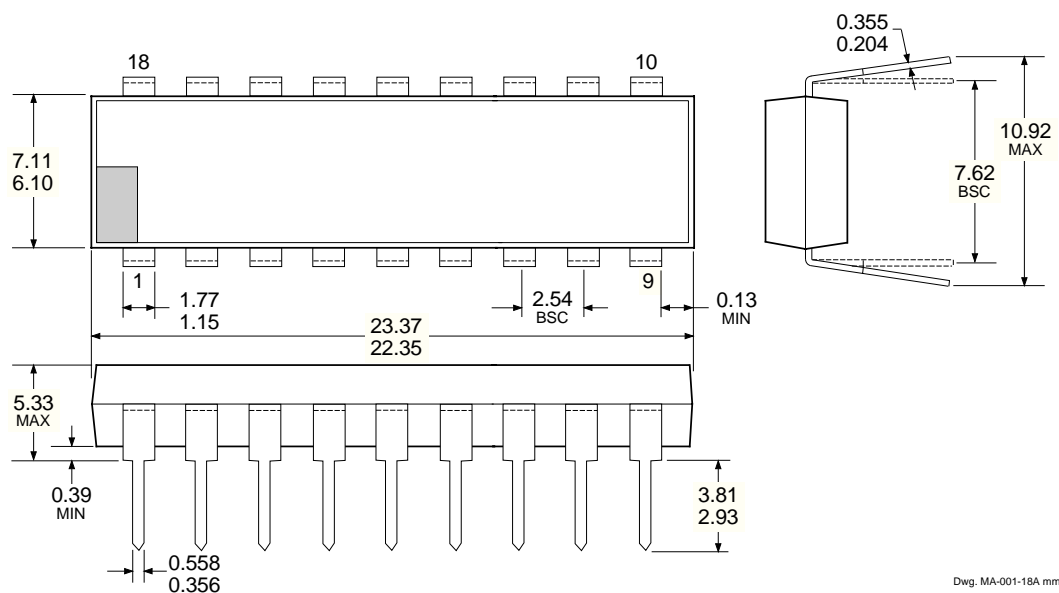
A6810EA, A6810KA, & A6810SA

Dimensions in Inches
(controlling dimensions)

18   10

0.280
0.240

1

0.070
0.045

0.100
BSC

9

0.005
MIN

0.920
0.880

0.210
MAX

0.015
MIN

0.022
0.014

0.150
0.115

0.014
0.008

0.430
MAX

0.300
BSC

Dwg. MA-001-18A in

Dimensions in Millimeters
(for reference only)

18   10

7.11
6.10

1

1.77
1.15

2.54
BSC

9

0.13
MIN

23.37
22.35

5.33
MAX

0.39
MIN

0.558
0.356

3.81
2.93

0.355
0.204
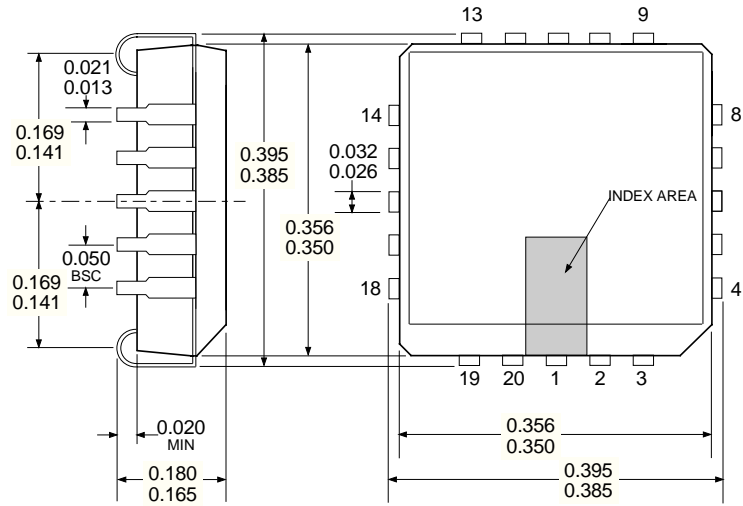
10.92
MAX

7.62
BSC

Dwg. MA-001-18A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
        2. Lead spacing tolerance is non-cumulative.
        3. Lead thickness is measured at seating plane or below.

A6810EEP, A6810KEP, & A6810SEP

Dimensions in Inches
(controlling dimensions)

13 9

14

INDEX AREA

8

18

4

19 20 1 2 3

0.021
0.013

0.169
0.141

0.395
0.385

0.032
0.026

0.356
0.350

0.050
BSC

0.169
0.141

0.020
MIN

0.180
0.165

0.356
0.350

0.395
0.385

Dwg. MA-005-20A in

Dimensions in Millimeters
(for reference only)

13 9

14

INDEX AREA

8

18

4

19 20 1 2 3

0.533
0.331

4.29
3.58

10.03
9.78

0.812
0.661

9.042
8.890

1.27
BSC
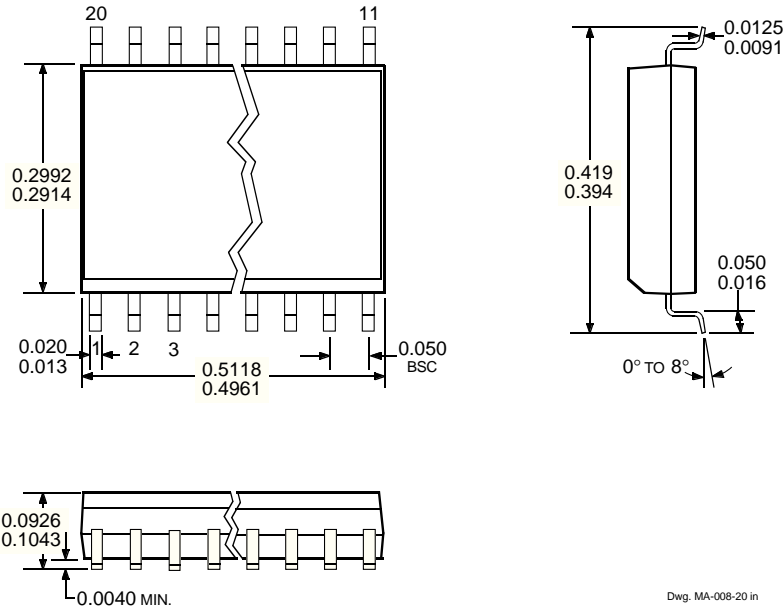
4.29
3.58

0.51
MIN

4.57
4.20

9.042
8.890

10.03
9.78
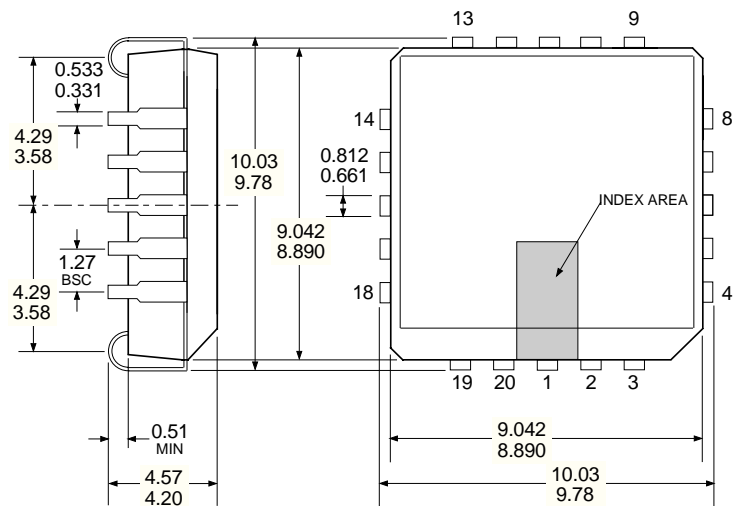
Dwg. MA-005-20A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
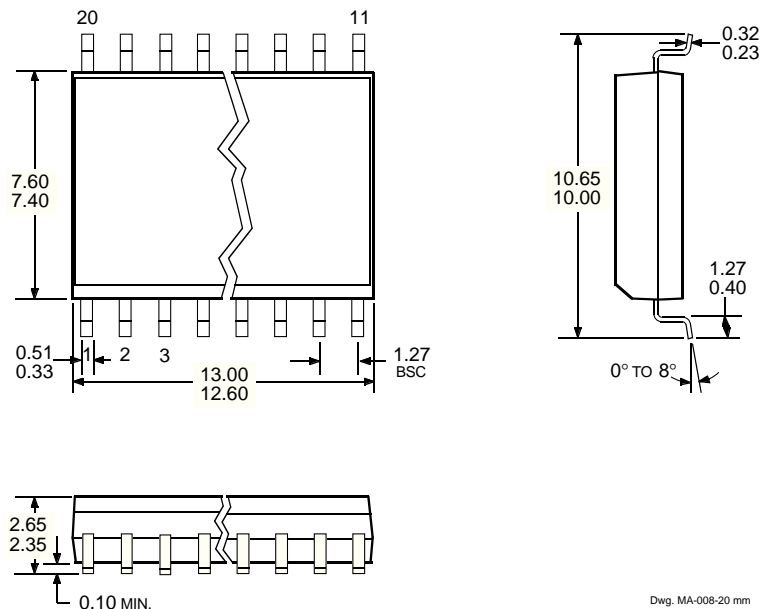2. Lead spacing tolerance is non-cumulative.

A6809ELW, A6809SLW, A6810ELW, A6810KLW, & A6810SLW

Dimensions in Inches
(for reference only)

20 11

0.2992
0.2914

0.020
0.013

1 2 3

0.5118
0.4961

0.050
BSC

0.0125
0.0091

0.419
0.394

0.050
0.016

0° TO 8°

0.0926
0.1043

0.0040 MIN.

Dwg. MA-008-20 in

Dimensions in Millimeters
(controlling dimensions)

20 11

7.60
7.40

0.51
0.33

1 2 3

13.00
12.60

1.27
BSC

0.32
0.23

10.65
10.00

1.27
0.40

0° TO 8°

2.65
2.35

0.10 MIN.

Dwg. MA-008-20 mm

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NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
     2. Lead spacing tolerance is non-cumulative.